(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 851 490 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
01.07.1998 Bulletin 1998/27

(51) Int. Cl.[6]: **H01L 23/522**, H01L 21/768

(21) Application number: **97122203.9**

(22) Date of filing: **16.12.1997**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **25.12.1996 JP 344721/96**

(71) Applicant: **NEC CORPORATION**
Tokyo (JP)

(72) Inventor: **Usami, Tatsuya**
Minato-ku, Tokyo (JP)

(74) Representative:
Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62
80058 München (DE)

(54) Semiconductor device and process for production thereof

(57) The present invention provides a semiconductor device comprising:

a semiconductor substrate having semiconductor elements, and
a plurality of wirings formed on the semiconductor substrate via an isolation film,
wherein the wirings are formed in at least one layer level so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region of large wiring-to-wiring distance; a first inter-level isolation film is selectively formed in the wiring region of small wiring-to-wiring distance and a second inter-level isolation film is formed in the wiring region of large wiring-to-wiring distance to cover the wirings; throughholes are formed only in the second inter-level isolation film; and the dielectric constant of the first inter-level isolation film is smaller than the dielectric constant of the second inter-level isolation film.

This semiconductor device has a fine multi-layered wiring structure of high performance and remarkably improved reliability.

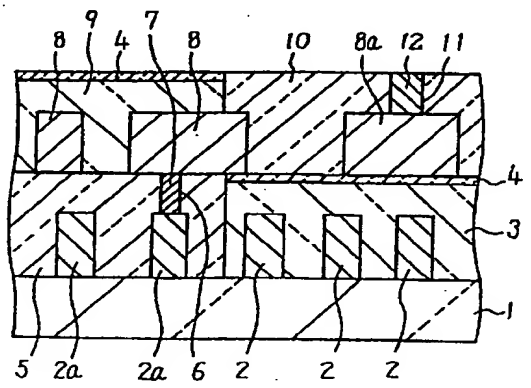

FIG.1

EP 0 851 490 A2

Description

BACKGROUND OF THE INVENTION

(i) Field of the Invention

The present invention relates to a semiconductor device and a process for production thereof. More particularly, the present invention relates to a fine wiring structure of semiconductor device and a process for production thereof.

(ii) Description of the Prior Art

As the semiconductor elements of semiconductor device become finer, the semiconductor device must have a finer multi-layered wiring structure. Currently, in semiconductor devices having such a multi-layered wiring structure, there is mainly used, as the inter-level isolation film, a silicon oxide-based isolation film of relatively small dielectric constant and stable quality so that the parasitic capacitance between upper-layer wirings and lower-layer wirings and between adjacent wirings in the same wiring layer level can be reduced.

As the semiconductor elements become finer, the wiring width and wiring-to-wiring distance of lower-layer wirings are made smaller; however, in order to avoid an increase in wiring resistance, the wirings in said wiring layer level must have a certain cross-sectional area. As a result, both the aspect ratio of a wiring (wiring height/wiring width) and the aspect ratio between wirings (wiring height/wiring-to-wiring distance) become large. This invites a significant increase in parasitic capacitance between wirings, resulting in (1) reduction in transfer speed of signal and (2) frequent occurrence of cross-talk between wiring layers (occurrence of signal noise between adjacent wirings).

Further, if the inter-level isolation film has a large step in the surface, when an upper wiring layer is formed, it is impossible to form a fine resist pattern by photolithography owing to the shortage of focus margin. Even if it is possible, the above-mentioned difference in surface level gives rise to (1) the wiring disconnection in upper-layer wirings and (2) remaining of unetched wiring material at the sites of level difference. Thus, the inter-level isolation film must have a flat surface.

In order to avoid the above-mentioned problems appearing in a fine multi-layered wiring structure, there have been proposed various techniques of using an inter-level isolation film of low dielectric constant. An example of such techniques is a technique disclosed in Japanese Patent Application Laid-Open No. 55913/1996. This technique is described below with reference to Fig. 7 and Fig. 8, both of which are sectional views showing the key production steps of the wiring structure used in the technique.

As shown in Fig. 7(a), a thick isolation film 101 is formed on a semiconductor substrate. On the thick isolation film 101 are formed a metal layer 102 and a first dielectric layer 103 in this order. On the first dielectric layer 103 is provided a resist mask 104. The first dielectric layer 103 is a highly reliable isolation film made of silicon oxide or the like.

Then, the first dielectric layer 103 and the metal layer 102 are subjected to reactive ion etching (RIE) by using the resist mask 104 as an etching mask. Thereafter, the remaining resist mask 104 is removed. Thus, as shown in Fig. 7(b), wirings 105 of small wiring-to-wiring distance and wirings 106 of large wiring-to-wiring distance are formed on the thick isolation film 101.

Next, as shown in Fig. 7(c), a low-dielectric constant material 107 is applied so as to cover the whole surfaces of the thick isolation film 101, the wirings 105 of small wiring-to-wiring distance, the wirings 106 of large wiring-to-wiring distance and the first dielectric layer 103, followed by levelling of the surface of the applied low-dielectric constant material. As the low-dielectric constant material 107, there is used, for example, a dielectric made of a polymer such as Teflon (trade mark), Parylene (trade mark) or the like.

On the whole surface of the low-dielectric constant material 107 is formed a hard oxide mask 108 as a resist layer. Then, the material 107 and the mask 108 are subjected to selectvie etching. That is, as shown in Fig. 8(a), the low-dielectric constant material 107 and the hard oxide mask 108 both in the region of wirings 106 of large wiring-to-wiring distance are removed and those in the region of wirings 105 of small wiring-to-wiring distance are allowed to remain.

Next, the hard oxide mask 108 on the region of the wirings 105 of small wiring-to-wiring distance is removed. As shown in Fig. 8(b), the low-dielectric constant material 107 is etched back and removed down to a level lower than the upper surface of the first dielectric layer 103 by dry etching. In that case, the first dielectric layer 103 functions as an etching stopper for the low-dielectric constant material 107. Preferably, the low-dielectric constant material 107 is not etched down to a level lower than the top of the wirings 105 of small wiring-to-wiring distance.

Next, as shown in Fig. 8(b), a second dielectric layer 109 is formed by deposition on the whole surface of the resulting material, that is, so as to cover the wirings 106 of large wiring-to-wiring distance, the first dielectric layer 103 and the etched-back low-dielectric constant material 107, then the surface of the second dielectric layer 109 is leveled. The second dielectric layer 109 is an isolation film made of silicon oxide or the like.

As above, on the thick isolation film 101 formed on a semiconductor substrate are formed lower-layer wirings and inter-level isolation films. In that case, a highly reliable isolation film made of silicon oxide or the like is formed in the region of large wiring-to-wiring distance, and a low-dielectric constant material is filled in the region of small wiring-to-wiring distance.

In forming a multi-layered wiring structure (this is not mentioned in the above literature), it is necessary to connect the lower-layer wirings formed by the prior art, with upper-layer wirings. In that case, as shown in Fig. 8(c), throughholes 110 and 110a are formed on a wiring 106 of large wiring-to-wiring distance and a wiring 105 of small wiring-to-wiring distance, respectively. Into the throughholes 110 and 110a are formed metal plugs 111 and 111a, respectively, and the lower-layer wirings and the upper-layer wirings are electrically connected with the metal plugs.

In the prior art as mentioned above, an isolation film of low-dielectric constant is selectively formed in the region of small wiring-to-wiring distance, of the wiring structure of semiconductor device. In this prior art, etching back of low-dielectric constant material 107 is necessary as mentioned with respect to Fig. 8(b). However, in the etching back, the etching-back depth of low-dielectric constant material is very difficult to control. It is also difficult to improve the uniformity of etching-back depth in a semiconductor wafer. Therefore, it is difficult to apply the prior art to production of a semiconductor having a fine wiring structure or using a semiconductor wafer of large diameter (e.g. diameter of 12 in.).

In the prior art, a first dielectric layer 103 and a second dielectric layer 109 are formed on or above both wirings 105 of small wiring-to-wiring distance and wirings 106 of large wiring-to-wiring distance. That is, no low-dielectric constant material 107 is formed on these wirings. Therefore, throughholes can be formed on these wirings. However, if mask alignment is deviated form the predetermined position as shown in Fig. 8(c) in the photolithography employed for throughhole formation, the low-dielectric constant material 107 is also etched in the region of wirings 105 of small wiring-to-wiring distance. When the low-dielectric constant material 107 is made of a polymer having a relative dielectric constant of 3 or less such as mentioned in the above-cited literature, the throughhole 110a formed in the region of wirings 105 of small wiring-to-wiring distance has a very disadvantageous shape. That is, the throughhole extends even to a direction perpendicular to the throughhole axial direction and comes to contain a void, whereby formation of a reliable metal plug 111a is difficult and the resulting semiconductor device has significantly reduced reliability.

SUMMARY OF THE INVENTION

The objects of the present invention are to provide a simple process for stably forming a fine wiring structure of semiconductor device; a fine multi-layered wiring structure of high performance and high reliability, of semiconductor device; and a process for forming such a fine multi-layered wiring structure.

According to the present invention, there is provided a semiconductor device comprising:

a semiconductor substrate having semiconductor elements, and

a plurality of wirings formed on the semiconductor substrate via an isolation film,

wherein the wirings are formed in at least one layer level so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region of large wiring-to-wiring distance; a first inter-level isolation film is selectively formed in the wiring region of small wiring-to-wiring distance and a second inter-level isolation film is formed in the wiring region of large wiring-to-wiring distance to cover the wirings; throughholes are formed only in the second inter-level isolation film; and the dielectric constant of the first inter-level isolation film is smaller than the dielectric constant of the second inter-level isolation film.

According to the present invention, there is also provided a semiconductor device comprising:

a semiconductor substrate having semiconductor elements, and

a plurality of wirings formed on the semiconductor substrate via an isolation film,

wherein the wirings are formed in at least one layer level so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region of large wiring-to-wiring distance; a first inter-level isolation film is selectively formed in the wiring region of small wiring-to-wiring distance, a second inter-level isolation film is formed in the wiring region of large wiring-to-wiring distance to cover the wirings; and a third inter-level isolation film is formed so as to cover the first inter-level-isolation film and the second inter-level isolation film; throughholes are formed only in the second inter-level isolation film and the third inter-level isolation film; and the dielectric constant of the first inter-level isolation film is smaller than the dielectric constants of the second inter-level isolation film and the third inter-level isolation film.

In each of the above semiconductors, it is preferable that the isolation film on the substrate is dented at the surface areas corresponding to the wiring region of small wiring-to-wiring distance but not covered by the wirings of the region and the resulting dents are filled with the first inter-level isolation film.

In each of the above semiconductors, the first inter-level isolation film is constituted by an organic film, an organic SOG film, a polyimide film, a porous inorganic SOG film having a density smaller than that of silicon oxide film, a porous organic SOG film, or a porous organic film, and the second inter-level isolation film is constituted by a silicon oxide film or a silicon oxynitride

film.

In each of the above semiconductors, when the wirings are formed in a multi-layered wiring structure, both the lower layer and the upper layer have the above-mentioned wiring structure.

According to the present invention, there is also provided a process for producing a semiconductor device, which comprises:

a step of forming a plurality of wirings on a semiconductor substrate via an isolation film so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region large wiring-to-wiring distance, and forming thereon a first inter-level isolation film so as to cover the wirings and then a protective isolation film in this order,
a step of selectively removing the first inter-level isolation film and the protective isolation film present on and in the wiring region of large wiring-to-wiring distance,
a step of forming, by deposition, a second inter-level isolation film on the whole surface of the resulting material and then subjecting the second inter-level isolation film to chemical mechanical polishing with the protective isolation film used as an etching stopper, to obtain a flat surface, and
a step of forming throughholes only in the second inter-level isolation film.

In the above process, the dielectric constant of the first inter-level isolation film is smaller than the dielectric constant of the second inter-level isolation film and the protective isolation film is more resistant to the chemical mechanical polishing than the second inter-level isolation film.

According to the present invention, there is also provided a process for producing a semiconductor device, which comprises:

a step of forming a plurality of wirings on a semiconductor substrate via an isolation film so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region large wiring-to-wiring distance, and forming thereon a second inter-level isolation film so as to cover the wirings,
a step of selectively removing the second inter-level isolation film present on and in the wiring region of small wiring-to-wiring distance,
a step of forming, by deposition, a first inter-level isolation film on the whole surface of the resulting material, and then subjecting the first inter-level isolation film to chemical mechanical polishing with the second inter-level isolation film used as an etching stopper to obtain a flat surface, and
a step of forming throughholes only in the second inter-level isolation film.

In the above process, the dielectric constant of the first inter-level isolation film is smaller than the dielectric constant of the second inter-level isolation film and the second inter-level isolation film is more resistant to the chemical mechanical polishing than the first inter-level isolation film.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view of a wiring region of semiconductor device, for explaining the first embodiment of the present invention.

Fig. 2 is sectional views showing the major production steps of the first embodiment of the present invention.

Fig. 3 is a plan view of a semiconductor device to which the present invention is applied.

Fig. 4 is a sectional view of a wiring region of semiconductor device, for explaining the second embodiment of the present invention.

Fig. 5 is sectional views showing the major production steps of the second embodiment of the present invention.

Fig. 6 is sectional views showing the major production steps of the second embodiment of the present invention.

Fig. 7 is sectional views showing the major production steps of the conventional semiconductor device, for explaining the prior art.

Fig. 8 is sectional views showing the production steps of the conventional semiconductor device, for explaining the prior art.

In Figs. 1-8;

1 is a base inter-level isolation film formed on a semiconductor substrate;
1a is a semiconductor chip;
2 and 2a are each a lower-layer wiring;
3 is a first inter-level isolation film;
4 is a protective isolation film;
5 and 5a are each a second inter-level isolation film;
6, 16, 110 and 110a are each a throughhole;
7, 111 and 111a are each a metal plug;
8 and 8a are each an upper-layer wiring;
9 is a first inter-level isolation film in upper layer;
10 and 10a are each a second inter-level isolation film in upper layer;
11 is a throughhole in upper layer;
12 is a metal plug in upper layer;
13 is a groove;
14 is a first inter-level isolation film;
15 is a second inter-level isolation film;
17 and 18 are each a third inter-level isolation film;
19 and 104 are each a resist mark;
101 is a thick isolation film;
102 is a metal layer;
103 is a first dielectric layer;
105 is a wiring in a wiring region of small wiring-to-

wiring distance;

106 is a wiring in a wiring region of large wiring-to-wiring distance;

107 is a low-dielectric constant material;

108 is a hard oxide mask; and

109 is a second dielectric layer.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention are described with reference to accompanying drawings. Fig. 1 is a sectional view of a wiring region of semiconductor device, for explaining the first embodiment of the present invention. Fig. 2 is sectional views showing the major steps employed in production of such a wiring region.

As shown in Fig. 1, a plurality of lower-layer wirings 2 and 2a are formed on a base inter-level isolation film 1 formed on a semiconductor substrate (e.g. a silicon substrate). The wirings 2 are formed in a wiring region of small wiring-to-wiring distance, and the wirings 2a are formed in a wiring region of large wiring-to-wiring distance. In the wiring region of small wiring-to-wiring distance, the distance between wirings is such that brings a noticeable increase in capacitance between wirings. This is usually less than 0.5 μm. On the other hand, in the wiring region of large wiring-to-wiring distance, the capacitance between wirings is not noticeably large. Where, the distance between wirings is usually more than or equal to 0.5 μm.

A first inter-level isolation film 3 is formed so as to fill the spacings between the wirings 2. On the first inter-level isolation film 3 is formed a protective isolation film 4. The base inter-level isolation film 1 is constituted by an ordinary silicon oxide film and has a relative dielectric constant of about 4.2. Meanwhile, the first inter-level isolation film 3 is constituted by an organic SOG film or the like and its relative dielectric constant is determined to be smaller than the relative dielectric constant of the isolation film 1. The protective isolation film 4 is constituted by an inorganic substance and, as will be mentioned later, functions as an etching stopper for the first inter-level isolation film 3.

In the region of wirings 2a having a large wiring-to-wiring distance is formed a second inter-level isolation film 5 as an inter-level isolation film. The second inter-level isolation film 5 is constituted by an isolation film of high moisture resistance and high quality. The film 5 is, for example, a silicon oxide film formed by chemical vapor deposition (CVD). In the given portions of the second inter-level isolation film 5 are formed throughholes 6. In each throughhole 6 is filled a metal plug 7, whereby electrical connection holds between the metal plug 7 and a wiring 2a.

No throughhole is formed in the first inter-level isolation film 3 made of a low-dielectric constant material and the protective isolation film 4 formed thereon.

An upper-layer wiring structure is formed in a manner similar to that used in formation of the lower-layer wiring structure. That is, on isolation films such as the protective isolation film 4, the second inter-level isolation film 5 and the like are formed upper-layer wirings 8a and 8, etc., and an upper-layer wiring 8 is connected with the metal plug 7. In the spacings between the upper-layer wirings 8 is filled a first inter-layer isolation film 9 made of a low-dielectric constant material and, on the first inter-level isolation film 9 is formed a protective isolation film 4. In the region of wirings 8a is formed a second inter-level isolation film 10 as an inter-level isolation film. The second inter-level isolation film 10, similarly to the second-inter level isolation film 5, is constituted by an isolation film of high moisture resistance and high quality. In the given portions of the second inter-level isolation film 10 are formed throughholes 11. In each throughhole 11 is filled a metal plug 12.

In the above formation of an upper-layer wiring strucure, the first inter-level isolation film 9 is formed on the second inter-level isolation film 5, and the second inter-level isolation film 10 is formed on the protective isolation film 4. The above constitution may be reversed. That is, the first inter-level isolation film 9 may be formed on the protective isolation film 4, and the second inter-level isolation film 10 may be formed on the second inter-level isolation film 5.

As described above, the feature of the wiring structure according to the first embodiment lies in that a first inter-level isolation film (which is a low dielectric constant isolation film) is formed in each wiring region of small wiring-to-wiring distance, a second inter-level isolation film of high moisture resistance and high quality is formed in each wiring region of large wiring-to-wiring distance and that throughholes are formed only in each second inter-level isolation film.

Next, description is made on the key steps employed in production of the above-mentioned wiring structure, with reference to Fig. 2. As shown in Fig. 2(a), a base inter-level isolation film 1 made of silicon oxide or the like is formed on a semiconductor substrate. On the isolation film 1 is deposited a metal by sputtering, to form a metal film. The metal film is an alloy film made of aluminum copper (AlCu) or the like and has a thickness of about 400 nm. The metal film may also be a laminated metal film made of, for example, Ti, TiN and AlCu.

Next, the metal film is subjected to fine processing by photolithography and dry etching to form lower-layer wirings 2 and 2a. The wirings 2 are wirings constituting a wiring region of small wiring-to-wiring distance, and the wirings 2a are wirings constituting a wiring region of large wiring-to-wiring distance.

On the whole surfaces of the isolation film 1 and the wirings 2 and 2a is formed a low-dielectric constant film, for example, by spin-coating, on the whole surfaces, a coating solution capable of forming an organic SOG film. The coating solution is filled over the wirings 2 and 2a. Then, a heat treatment is applied to heat-cure the solution and form an organic SOG film. The organic

SOG film has a relative dielectric constant of 3 or less. The organic SOG film is subjected to chemical mechanical polishing (CMP) for levelling, whereby a first inter-level isolation film 3 as shown in Fig. 2(a) is formed. The first inter-level isolation film 3 is controlled so as to have a thickness of about 600 nm.

Next, on the first inter-level isolation film 3 is formed a protective isolation film 4. The protective isolation film 4 is formed by plasma CVD, is made of silicon nitride, silicon oxynitride or silicon carbide, and is controlled so as to have a thickness of about 50 nm.

Next, as shown in Fig. 2(b), photolithography and dry etching are applied to remove the protective isolation film 4 and the first inter-level isolation film 3 so that the portions of the film 4 and the film 3 both present in the region of wirings 2 are allowed to remain.

Next, a second inter-level isolation film 5 is formed by deposition so as to cover the wirings 2a and the protective isolation film 4. The second inter-level isolation film 5 is formed by plasma CVD using bias ECR, is made of silicon oxide, and has a thickness of about 800 nm.

Next, the second inter-level isolation film in a Fig. 2(b) state is levelled by CMP, as shown in Fig. 2(c). In this CMP, the protective isolation film 4 functions as an etching stopper. That is, by using an abrasive with which a silicon oxide film is selectively polished and to which a silicon nitride film or a silicon oxynitride film is resistant to polishing, the second inter-level isolation film 5 is polished selectively and the first inter-level isolation film 3 is protected from polishing owing to the presence of the protective isolation film 4. Further, the protective isolation film 4 can significantly improve the film thickness uniformity of the second inter-level isolation film 5 after polishing.

Next, throughholes 6 are formed in the given portions of the second inter-level isolation film 5, and a metal plug 7 is filled in each throughhole 7. The metal plug 7 is formed, for example, by formation of a tungsten film by CVD and polishing thereof by CMP.

Thus, a lower-layer wiring structure is formed. Thereon is formed an upper-layer wiring structure as mentioned with respect to Fig. 1. The process for formation of an upper-layer wiring structure is similar to the above-mentioned process for formation of a lower-layer wiring structure and, therefore, is not mentioned.

As the first inter-layer isolation film 3, there maybe used a hygroscopic organic isolation film (e.g. a polyimide film), a porous inorganic SOG film having a density smaller than that of silicon oxide film, a porous organic SOG film or the like. Or, there may be used an inorganic isolation film such as SiOF film, SiBN film or the like.

One of the features of the wiring structure of the present invention lies in that a low-dielectric constant isolation film is selectively formed in each wiring region of small wiring-to-wiring distance, an inter-level isolation film of high moisture resistance and high quality is formed in each wiring region of large wiring-to-wiring distance and that throughholes are formed only in each inter-level isolation film of high moisture resistance and high quality. This feature is explained with reference to Fig. 3. Fig. 3 is a plan view of a semiconductor device to which the present invention is applied.

As shown in Fig. 3, a first inter-level isolation film 14 (which is a low-dielectric constant isolation film) is selectively formed on the given areas of a semiconductor chip 1a. Thereby, the parasitic capacitance between adjacent wirings is reduced and the transfer speed of signal is increased.

Further, a second inter-level isolation film 15 (which is an isolation film of high moisture resistance and high quality) is formed on an area of the semiconductor chip 1a. Throughholes 16 for connecting a lower wiring layer and an upper wiring layer are formed in the second inter-level isolation film 15. In each throughhole, a metal plug is filled.

In general, a low-dielectric constant isolation film has a large thermal expansion coefficient, a small strength and high hygroscopy. The hygroscopy becomes higher as the dielectric constant becomes smaller.

Therefore, when throughholes are formed in a low-dielectric constant isolation film, the electrical resistance of connections between lower-layer wirings and upper-layer wirings via these throughholes changes with the lapse of time. That is, the reliability of wirings decreases largely with the lapse of time. For example, the electrical resistance comes to increase due to the presence of moisture and resulting corrosion of wirings communicating with the throughholes or fluorination of aluminum metal. Such quality deterioration is more striking when the wiring structure has more layers. Due to such reduction in reliability of wiring structure, the dielectric constant of inter-level isolation film are not able to be lowered beyond a certain limit.

In contrast, in the above-mentioned embodiment of the present invention, throughholes are formed only in the second inter-level isolation film of high moisture resistance and high quality. Therefore, a multi-layered wiring structure of high performance and high reliability is made possible.

Next, description is made on the second embodiment of the present invention. Fig. 4 is a sectional view of a wiring portion of semiconductor device, for explaining the second embodiment of the present invention. Fig. 5 and Fig. 6 are sectional views showing the major steps employed in production of such a wiring portion. In Figs. 4 to 6, members having the same functions as in the first embodiment are shown by the same symbols.

As shown in Fig. 4, a plurality of lower-layer wirings 2 and 2a are formed on a base inter-levvel isolation film 1 formed on a semiconductor substrate. In the surface areas of the isolation film 1 present between the wirings 2 are formed grooves 13. The wirings 2 are wirings of a wiring region of small wiring-to-wiring distance, and the wirings 2a are wirings of a wiring region of large wiring-

to-wiring distance.

A first inter-level isolation film 3 is formed so as to fill the gaps between the wirings 2 and the grooves 13. The isolation film 1 is constituted by an ordinary silicon oxide film. Meanwhile, the first inter-level isolation film 3 is constituted by an organic SOG film or the like.

In the region of the wirings 2a having a large wiring-to-wiring distance is formed a second inter-level isolation film 5a as an inter-level isolation film. The second inter-level isolation film 5a is constituted by an isolation film of high moisture resistance and high quality which is made of an insulating material different from that used in the first inter-level isolation film 3. The isolation film 5a is, for example, a silicon oxynitride film formed by CVD.

A third inter-level isolation film 17 is formed so as to cover the first inter-level isolation film 3 and the second inter-level isolation film 5a. The third inter-level isolation film 17, similarly to the second inter-level isolation film 5a, is constituted by an isolation film of high moisture resistance and high quality.

In the given portions of the second inter-level isolation film 5a and the third inter-level isolation film 17 are formed throughholes 6. In each throughhole 6 is filled a metal plug 7, whereby electrical connection between plug and lower-layer wiring 2a is achieved.

Similarly to the case of the first embodiment, no throughhole is formed in the first inter-level isolation film 3 constituted by a low-dielectric constant isolation film.

An upper wiring layer is formed in a manner similar to that used in formation of a lower wiring layer. That is, upper-layer wirings 8a and 8, etc. are formed on the third inter-level isolation film 17, whereby electrical connection between upper-layer wiring 8 and metal plug 7 is achieved. In the surface areas of the isolation film 17 present between the wirings 8 are formed grooves 13. Between the wirings 8 and in the grooves 13 is filled a first inter-level isolation film 9 constituted by a low-dielectric constant isolation film. In the region of the wirings 8a having a large wiring-to-wiring distance is formed a second inter-level isolation film 10a as an inter-level isolation film. A third inter-level isolation film 18 is formed so as to cover the whole surfaces of isolation films 9 and 10a. The second inter-level isolation film 10a and the third inter-level isolation film 18 are each constituted by an isolation film of high moisture resistance and high quality. In the given portions of the second inter-level isolation film 10a and the third inter-level isolation film 18 are formed throughholes 11. In each throughhole 11 is filled a metal plug 12.

In the above-mentioned formation of an upper wiring layer, the first inter-level isolation film 9 is formed on the second inter-level isolation film 5a, and the second inter-level isolation film 10a is formed on the first inter-level isolation film 3. The above constitution may be reversed. That is, the first inter-level isolation film 9 is formed on the first inter-level isolation film 3, and the second inter-level isolation film 10a is formed on the second inter-level isolation film 5a.

As described above, the feature of the wiring structure according to the second embodiment of the present invention lies in that grooves of certain depth are formed at the surface areas of each isolation film present at the bottom of each wiring level, corresponding to each wiring region of small wiring-to-wiring distance but not covered by the wirings of the region. A low-dielectric constant isolation film is formed so as to fill not only between the wirings of the region but also the grooves. As a result, the parasitic capacitance between adjacent wirings due to the fringe effect is greatly reduced. This merit is more striking in a finer wiring structure.

The process for producing the above-mentioned wiring structure is described with reference to Fig. 5 and Fig. 6. As shown in Fig. 5(a), on a base inter-llevel isolation film 1 constituted by a silicon oxide film are formed lower-layer wirings 2 and 2a, in a manner similar to that mentioned in the first embodiment. The wirings 2 are wirings of a wiring region of small wiring-to-wiring distance, and the wirings 2a are wirings of a wiring region of large wiring-to-wiring distance. The wirings 2 and 2a have a line width of about 0.3 μm and a height of 0.4 μm.

Next, on the whole surfaces of the isolation film 1, the wirings 2 and the wirings 2a is formed a second inter-level isolation film 5a. The second inter-level isolation film 5a is a silicon oxynitride film formed by plasma CVD, and is levelled by CMP. On the surface area of the second inter-level isolation film 5a covering the wirings 2a is formed a resist mask 19. As shown in Fig. 5(b), by using the resist mask 19 as an etching mask, the second inter-level isolation film 5a in the wiring region of small wiring-to-wiring distance is subjected to anisotropic etching by RIE. In this case, even part of the surface of the isolation film 1 is etched by RIE and grooves 13 of the same pattern as the wirings 2 are formed. The depth of each groove is controlled similar to the line width of wiring 2. Then, the resist mask 19 is removed.

Next, as shown in Fig. 5(c), on the whole surfaces of the resulting material is formed a first inter-level isolation film 3. The first inter-level isolation film 3 is a low-dielectric constant isolation film constituted by, for example, an organic SOG film such as mentioned in the first embodiment. The thickness of the first inter-level isolation film 3 is controlled at about 600 nm.

Next, the first inter-level isolation film 3 in a Fig. 5(c) state is subjected to CMP for surface levelling, as shown in Fig. 6(a). In this polishing step, the second inter-level isolation film 5a functions as an etching stopper. That is, by using an abrasive with which the first inter-level isolation film constituted by an organic SOG film or the like is selectively polished and to which the second inter-level isolation film constituted by a silicon oxynitride film or the like has abrasion resistance, the first inter-level isolation film 3 is polished selectively.

Next, as shown in Fig. 6(b), a third inter-level isolation film 17 is formed on the levelled first inter-level isolation film 3 and the levelled second inter-level isolation

film 5a. The third inter-level isolation film 17 is a silicon oxide film formed by CVD and has a thickness of about 300 nm. Thus, a lower-layer wiring structure is formed. As the first inter-level isolation film 3, there may be used a hygroscopic organic isolation film (e.g. a polyimide film), a porous inorganic SOG film having a density smaller than that of silicon oxide film, a porous organic SOG film or the like. Or, an inorganic isolation film such as SiOF film, SiBN film or the like may be used. In these cases, a silicon oxide film may be used as the second inter-level isolation film 5a.

Next, as shown in Fig. 6(c), throughholes 6 are formed in the given portions of the second inter-level isolation film 5a and the third inter-level isolation film 17, both present in the wiring region of large wiring-to-wiring distance. In each throughhole 6 is filled a metal plug 7, whereby electrical connection between metal plug 7 and wiring 2a is achieved.

Next, an upper-layer wiring structure as mentioned with respect to Fig. 4 is formed. The process for formation of an upper-layer wiring structure is performed in the similar manner to the above-described process for formation of a lower, wiring layer.

In the second embodiment, each first inter-level isolation film formed in each wiring region of small wiring-to-wiring distance is filled even in the dents formed in each isolation film present beneath the wirings of the region. As a result, the parasitic capacitance generated between the bottom ends of adjacent wirings is reduced.

In the present invention, as the low-dielectric constant isolation film, there can be used, in addition to those films mentioned above in the embodiments, films of HSQ (hydrogen silsesquioxane), polyaryl ether, fluorinated polyaryl ether, inorganic polysilazane, organic polysilazane, BCB (benzocyclobutene), MSQ (methyl silsesquioxane), fluorinated polyimide, plasma CF polymer, plasma CH polymer, Teflon AF (trade mark), Parylene N (trade mark), AF-4 (polyparaxylylene), Polynaphthalene N, etc.

As described above, in each wiring layer level of the semiconductor of the present invention, an inter-level isolation film of low dielectric constant is formed in the region of small wiring-to-wiring distance and an inter-level isolation film of high moisture resistance and high quality is formed in the region of large wiring-to-wiring distance; and throughholes for connecting lower-layer wirings and upper-layer wirings are formed only in the inter-level isolation film of high moisture resistance and high quality.

Further, in polishing and levelling of the first inter-level isolation film by CMP, the second inter-level isolation film is used as an etching stopper.

As a result, the reliability of connection between lower-layer wirings and upper-layer wirings is greatly improved and a fine multi-layered wiring structure is made possible. Further, the film thickness uniformity of the first inter-level isolation 3 on a semiconductor chip is greatly improved.

Further in the present invention, grooves of certain depth are formed at the surface areas of each isolation film present at the bottom of each wiring layer, corresponding to each wiring region of small wiring-to-wiring distance but not covered by the wirings of the region, and a low-dielectric constant film is formed so as to fill not only the spacings between the wirings of said region but also the grooves.

As a result, the parasitic capacitance between adjacent wirings due to the fringe effect is greatly reduced. This merit is more striking in a finer wiring structure.

Thus, there is easily obtained a fine multi-layered wiring structure of high performance and high reliability, required in a fine and multifunctional semiconductor device.

Claims

1. A semiconductor device comprising:

   a semiconductor substrate having semiconductor elements, and
   a plurality of wirings formed on the semiconductor substrate via an isolation film,
   wherein the wirings are formed in at least one layer level so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region of large wiring-to-wiring distance; a first inter-level isolation film is selectively formed in the wiring region of small wiring-to-wiring distance and a second inter-level isolation film is formed in the wiring region of large wiring-to-wiring distance to cover the wirings; throughholes are formed only in the second inter-level isolation film; and the dielectric constant of the first inter-level isolation film is smaller than the dielectric constant of the second inter-level isolation film.

2. A semiconductor device according to Claim 1, comprising:

   a semiconductor substrate having semiconductor elements, and
   a plurality of wirings formed on the semiconductor substrate via an isolation film,
   wherein the wirings are formed in at least one layer level so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region of large wiring-to-wiring distance; a first inter-level isolation film is selectively formed in the wiring region of small wiring-to-wiring distance, a second inter-level isolation film is formed in the wiring region of large wiring-to-wiring distance to cover the wirings; and a third

inter-level isolation film is formed so as to cover the first inter-level-isolation film and the second inter-level isolation film; throughholes are formed only in the second inter-level isolation film and the third inter-level isolation film; and the dielectric constant of the first inter-level isolation film is smaller than the dielectric constants of the second inter-level isolation film and the third inter-level isolation film.

3. A semiconductor device according to Claim 1, wherein the isolation film on the substrate is dented at the surface areas corresponding to the wiring region of small wiring-to-wiring distance but not covered by the wirings of the region and the resulting dents are filled with the first inter-level isolation film.

4. A semiconductor device according to Claim 2, wherein the isolation film on the substrate is dented at the surface areas corresponding to the wiring region of small wiring-to-wiring distance but not covered by the wirings of the region and the resulting dents are filled with the first inter-level isolation film.

5. A semiconductor device according to Claim 1, wherein the first inter-level isolation film is constituted by an organic film, an organic SOG film, a polyimide film, a porous inorganic SOG film having a density smaller than that of silicon oxide film, or a porous organic SOG film, and the second inter-level isolation film is constituted by a silicon oxide film or a silicon oxynitride film.

6. A semiconductor device according to Claim 2, wherein the first inter-level isolation film is constituted by an organic film, an organic SOG film, a polyimide film, a porous inorganic SOG film having a density smaller than that of silicon oxide film, or a porous organic SOG film, and the second inter-level isolation film is constituted by a silicon oxide film or a silicon oxynitride film.

7. A semiconductor device according to Claim 1, wherein the wirings are formed in a plurality of layer levels so that at each layer level the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region of large wiring-to-wiring distance; a first inter-level isolation film is selectively formed in the wiring region of small wiring-to-wiring distance and a second inter-level isolation film is formed in the wiring region of large wiring-to-wiring distance to cover the wirings; through-holes are formed only in the second inter-level isolation film; and the dielectric constant of the first inter-level isolation film is smaller than the dielectric constant of the second inter-level isolation film.

8. A semiconductor device according to Claim 2, wherein the wirings are formed in a plurality of layer levels so that at each layer level the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region of large wiring-to-wiring distance; a first inter-level isolation film is selectively formed in the wiring region of small wiring-to-wiring distance, a second inter-level isolation film is formed in the wiring region of large wiring-to-wiring distance to cover the wirings; and a third inter-level isolation film is formed so as to cover the first inter-level isolation film and the second inter-level isolation film; throughholes are formed only in the second inter-level isolation film and the third inter-level isolation film; and the dielectric constant of the first inter-level isolation film is smaller than the dielectric constants of the second inter-level isolation film and the third inter-level isolation film.

9. A semiconductor device according to Claim 7, wherein the isolation film on the substrate is dented at the surface areas corresponding to the wiring region of small wiring-to-wiring distance but not covered by the wirings of the region and the resulting dents are filled with the first inter-level isolation film.

10. A semiconductor device according to Claim 8, wherein the isolation film on the substrate is dented at the surface areas corresponding to the wiring region of small wiring-to-wiring distance but not covered by the wirings of the region and the resulting dents are filled with the first inter-level isolation film.

11. A semiconductor device according to Claim 7, wherein the first inter-level isolation film is constituted by an organic film, an organic SOG film, a polyimide film, a porous inorganic SOG film having a density smaller than that of silicon oxide film, or a porous organic SOG film, and the second inter-level isolation film is constituted by a silicon oxide film or a silicon oxynitride film.

12. A semiconductor device according to Claim 8, wherein the first inter-level isolation film is constituted by an organic film, an organic SOG film, a polyimide film, a porous inorganic SOG film having a density smaller than that of silicon oxide film, or a porous organic SOG film, and the second inter-level isolation film is constituted by a silicon oxide film or a silicon oxynitride film.

13. A process for producing a semiconductor device, which comprises:

a step of forming a plurality of wirings on a semiconductor substrate via an isolation film so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region large wiring-to-wiring distance, and forming thereon a first inter-level isolation film so as to cover the wirings and then a protective isolation film in this order,

a step of selectively removing the first inter-level isolation film and the protective isolation film present on and in the wiring region of large wiring-to-wiring distance,

a step of forming, by deposition, depositing a second inter-level isolation film on the whole surface of the resulting material and then subjecting the second inter-level isolation film to chemical mechanical polishing with the protective isolation film used as an etching stopper, to obtain a flat surface, and

a step of forming throughholes only in the second inter-level isolation film.

14. A process according to Claim 13, wherein the dielectric constant of the first inter-level isolation film is smaller than the dielectric constant of the second inter-level isolation film and the protective isolation film is more resistant to the chemical mechanical polishing than the second inter-level isolation film.

15. A process according to Claim 14, wherein the protective isolation film is constituted by a silicon nitride film, a silicon oxynitride film or a silicon carbide film and the second inter-level isolation film is constituted by a silicon oxide film.

16. A process for producing a semiconductor device, which comprises:

a step of forming a plurality of wirings on a semiconductor substrate via an isolation film so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region large wiring-to-wiring distance, and forming thereon a second inter-level isolation film so as to cover the wirings,

a step of selectively removing the second inter-level isolation film present on and in the wiring region of small wiring-to-wiring distance,

a step of forming, by deposition, depositing a first inter-level isolation film on the whole surface of the resulting material, and then subjecting the first inter-level isolation film to chemical mechanical polishing with the second inter-level isolation film used as an etching stopper to obtain a flat surface, and

a step of forming throughholes only in the second inter-level isolation film.

17. A process according to Claim 16, wherein the dielectric constant of the first inter-level isolation film is smaller than the dielectric constant of the second inter-level isolation film and the second inter-level isolation film is more resistant to the chemical mechanical polishing than the first inter-level isolation film.

18. A process according to Claim 17, wherein the first inter-level isolation film is constituted by an organic film, an organic SOG film, a polyimide film, a porous inorganic SOG film having a density smaller than that of silicon oxide film, or a porous organic SOG film, and the second inter-level isolation film is constituted by a silicon oxide film or a silicon oxynitride film.

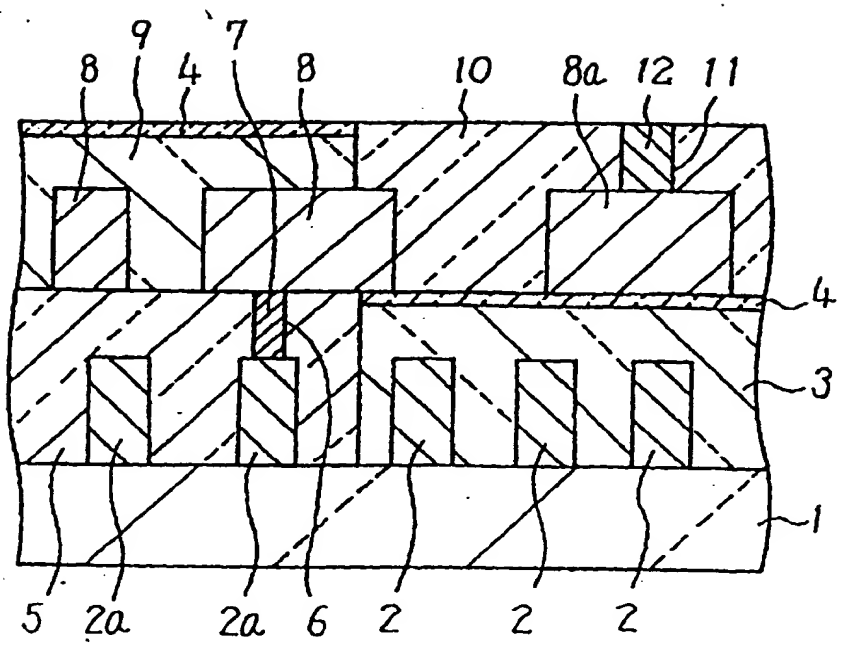

FIG.1

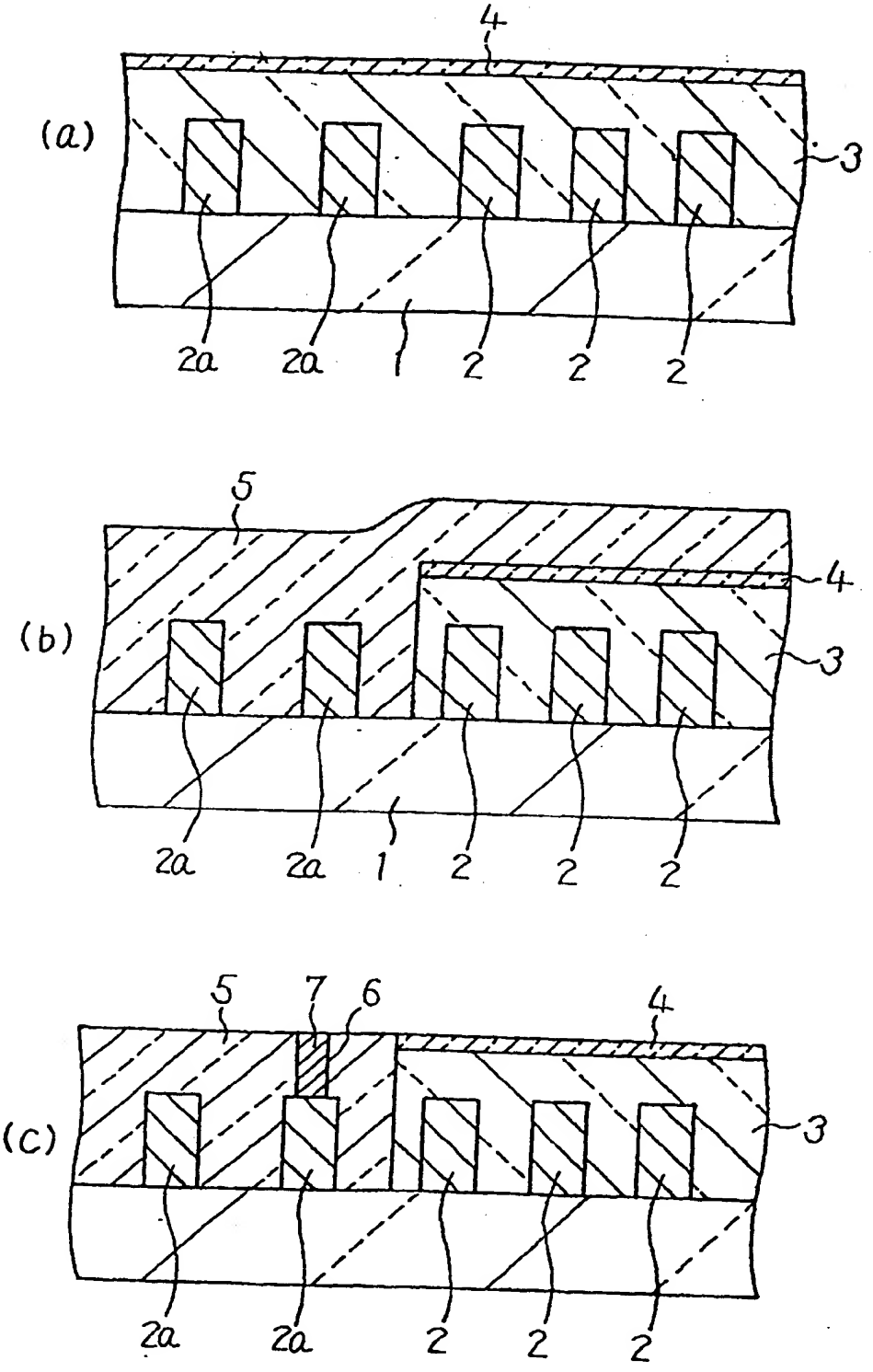

FIG.2

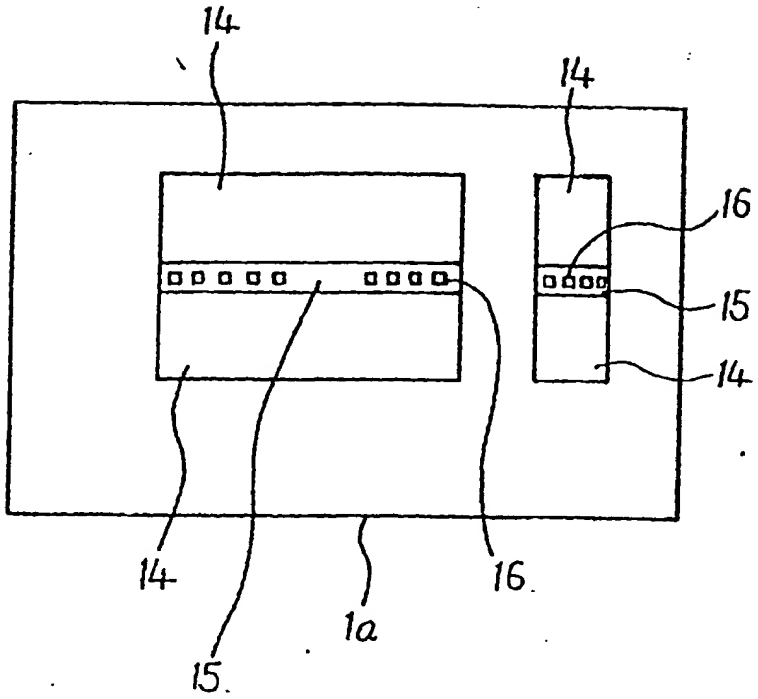

FIG.3

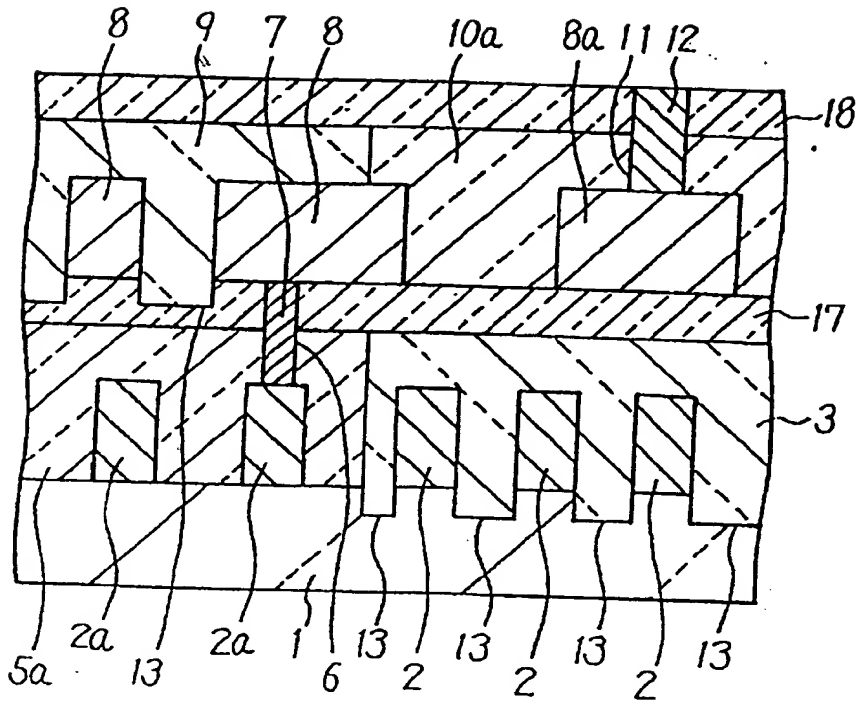

FIG.4

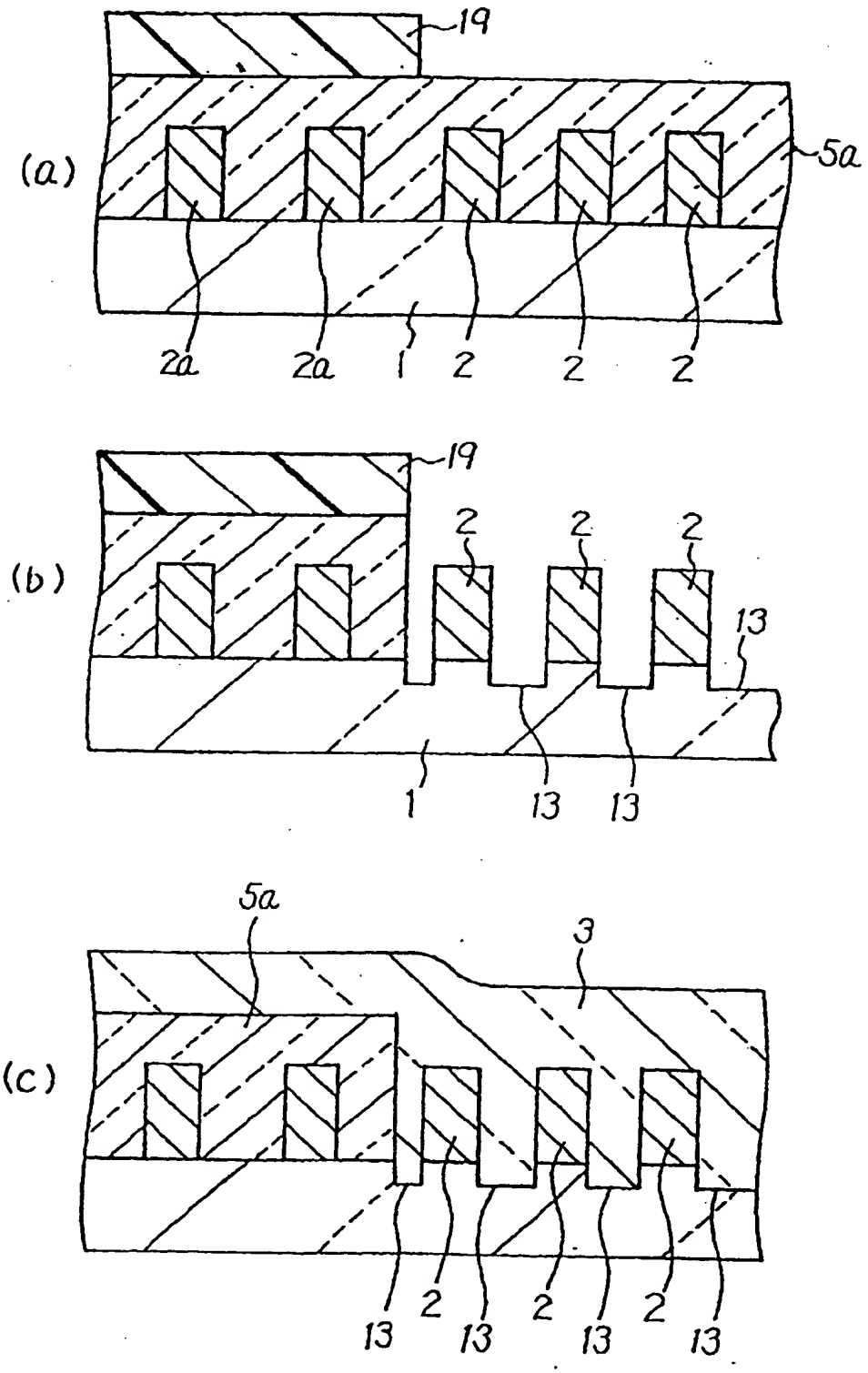

FIG.5

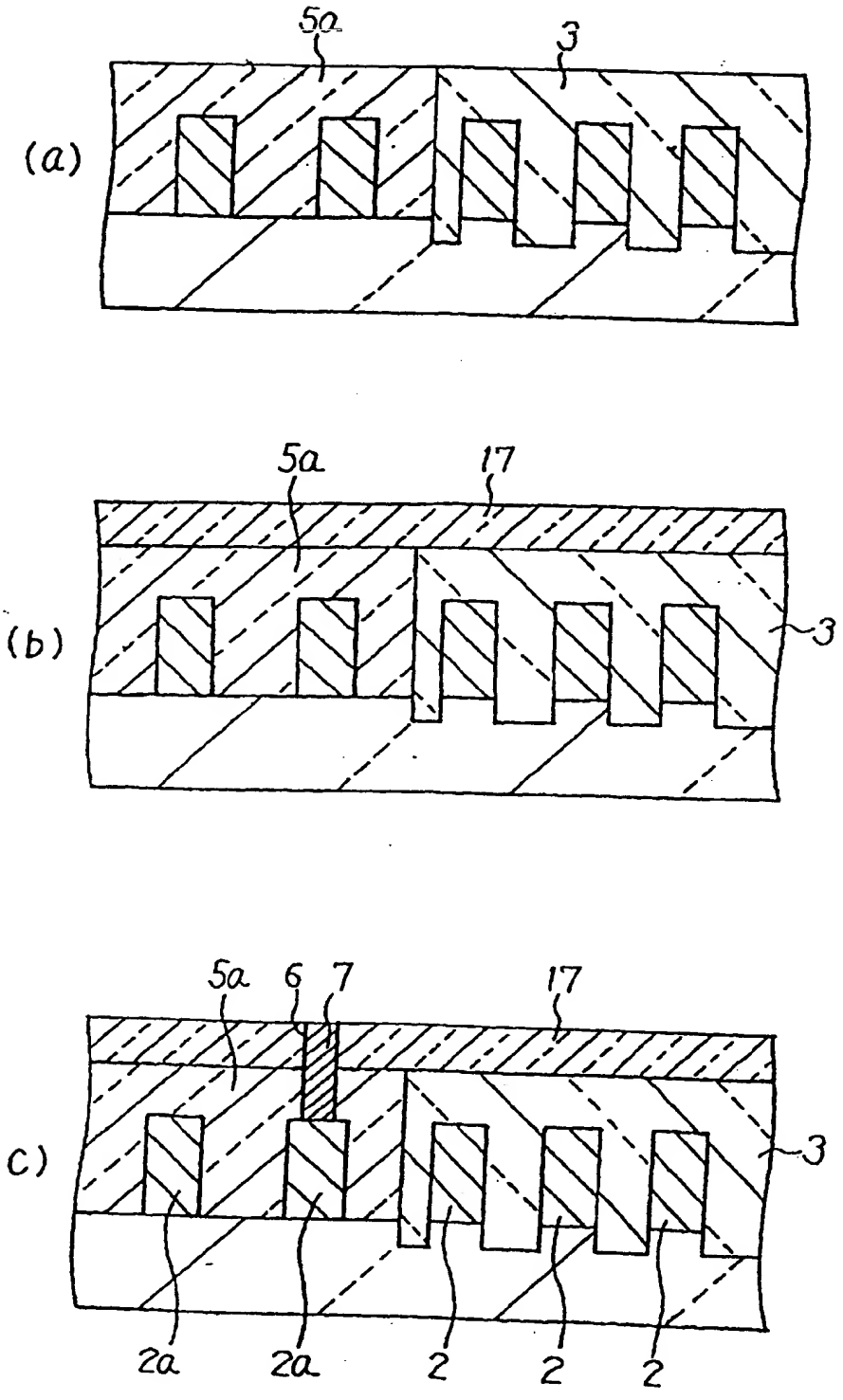

FIG.6

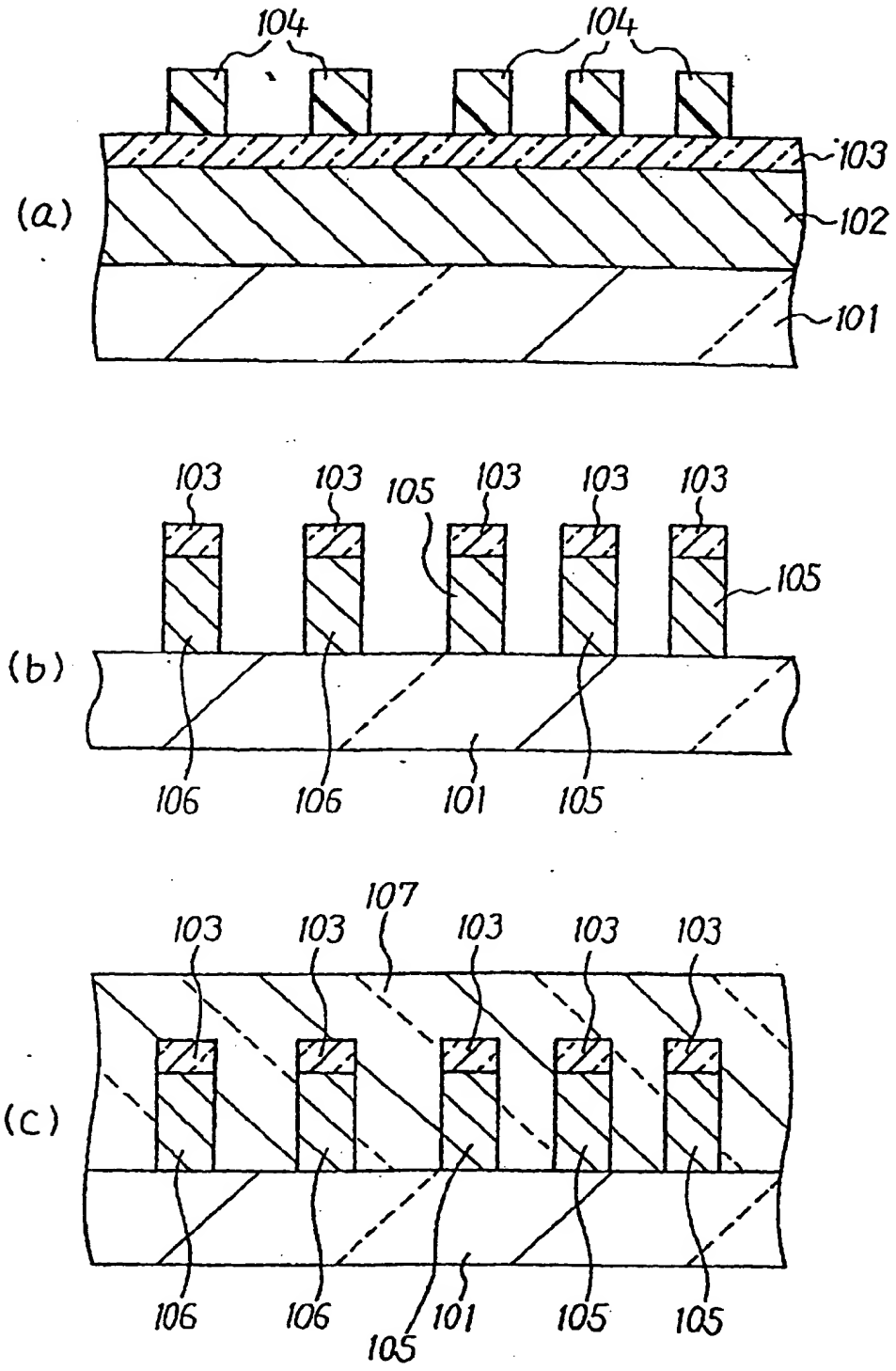

FIG.7

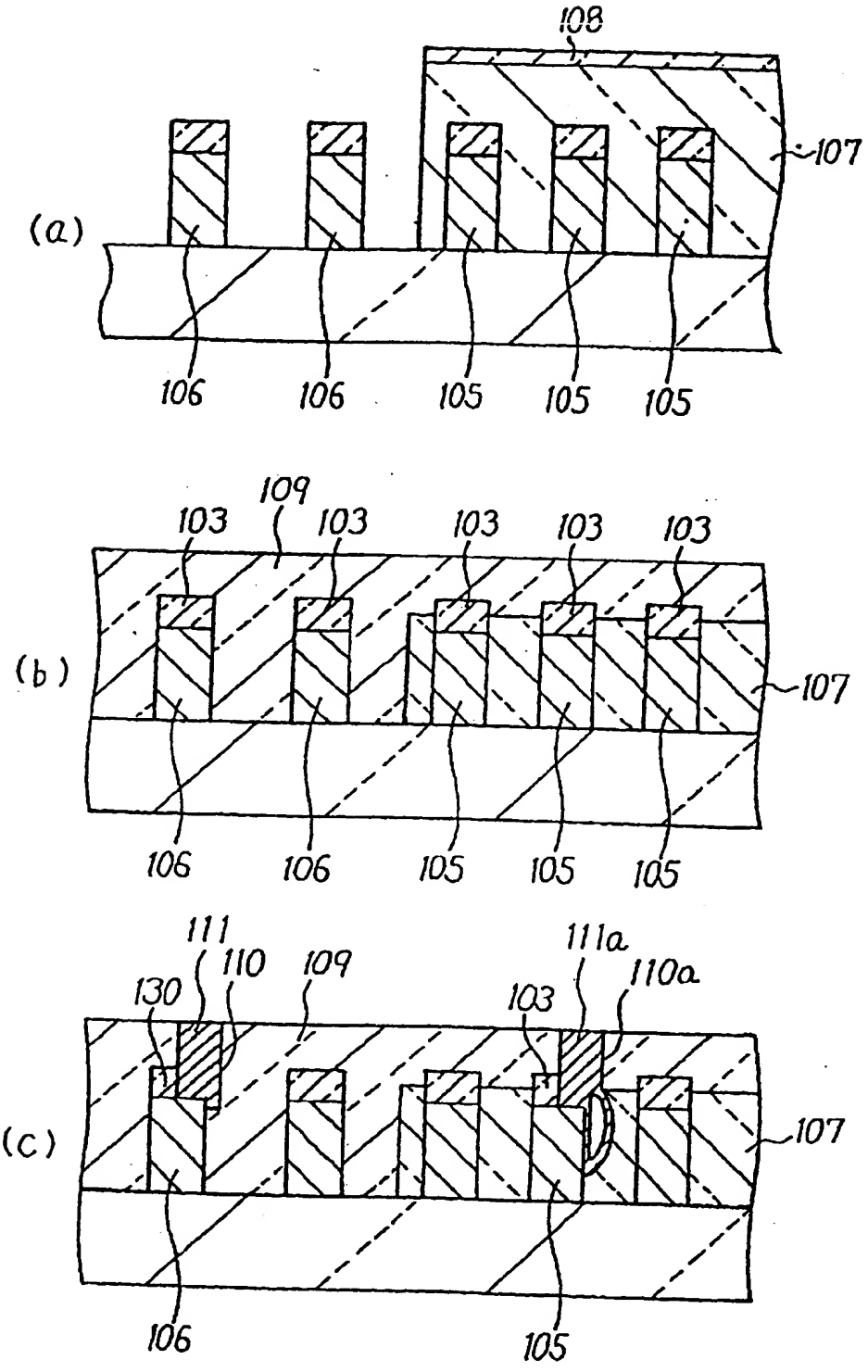

FIG.8

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 851 490 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
22.12.1999 Bulletin 1999/51

(43) Date of publication A2:
01.07.1998 Bulletin 1998/27

(21) Application number: **97122203.9**

(22) Date of filing: **16.12.1997**

(51) Int. Cl.[6]: **H01L 23/522**, H01L 21/768, H01L 23/532

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **25.12.1996 JP 34472196**

(71) Applicant: **NEC CORPORATION**
Tokyo (JP)

(72) Inventor: **Usami, Tatsuya**
Minato-ku, Tokyo (JP)

(74) Representative:
Glawe, Delfs, Moll & Partner
Patentanwälte
Postfach 26 01 62
80058 München (DE)

(54) Semiconductor device and process for production thereof

(57) A semiconductor substrate (1A) having semiconductor elements, and

a plurality of wirings (2,2A) formed on the semiconductor substrate via an isolation film (1),
wherein the wirings are formed in at least one layer level so that the region in which the wirings are formed is divided into a wiring region of small wiring-to-wiring distance and a wiring region of large wiring-to-wiring distance; a first inter-level isolation film is selectively formed in the wiring region of small wiring-to-wiring distance and a second inter-level isolation film is formed in the wiring region of large wiring-to-wiring distance to cover the wirings; throughholes are formed only in the second inter-level isolation film; and the dielectric constant of the first inter-level isolation film is smaller than the dielectric constant of the second inter-level isolation film.

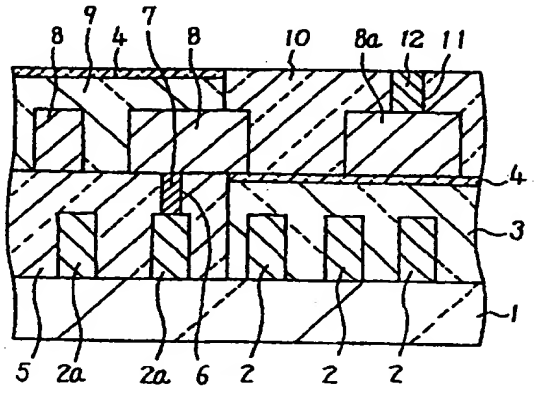

FIG.1

EP 0 851 490 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 12 2203

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
E	EP 0 805 491 A (TEXAS INSTRUMENTS INC) 5 November 1997 (1997-11-05) * column 6, line 15-52; figures 4A-C *	1,5-8	H01L23/522 H01L21/768 H01L23/532
X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 07, 31 March 1999 (1999-03-31) -& JP 08 195437 A (TEXAS INSTR INC <TI>), 30 July 1996 (1996-07-30) * abstract *	1,5,7,11	
A	EP 0 706 216 A (SONY CORP) 10 April 1996 (1996-04-10) * page 4, line 55 - page 5, line 26; figure 3 *	3,4,9,10	
D,A	EP 0 687 005 A (TEXAS INSTRUMENTS INC) 13 December 1995 (1995-12-13) * figures 2A-2D *	1-18	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	26 October 1999	Edmeades, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 97 12 2203

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

26-10-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0805491 A	05-11-1997	JP 10041382 A	13-02-1998
JP 08195437 A	30-07-1996	NONE	
EP 0706216 A	10-04-1996	JP 8162528 A	21-06-1996
		US 5646440 A	08-07-1997
EP 0687005 A	13-12-1995	JP 8055913 A	27-02-1996
		US 5789319 A	04-08-1998
		US 5786624 A	28-07-1998

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82